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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KARSTEN WIECZOREK, THOMAS FEUDEL, THORSTEN KAMMLER and WOLFGANG BUCHHOLTZ

Appeal 2007-3852
Application 10/790,852
Technology Center 2800

Decided: September 4, 2008

Before KENNETH W. HAIRSTON, SCOTT R. BOALICK,
and KEVIN F. TURNER, *Administrative Patent Judges*.
HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. §§ 6(b) and 134 from the final rejection of claims 1 to 15 and 21 to 32.

The disclosed invention relates to a method of making the drain and the source regions on the top surface of a crystalline semiconductor region. The drain and source regions are formed adjacent an implantation mask on the crystalline semiconductor region. After formation of the drain and source regions, the implantation mask is removed to expose the top surface of the crystalline semiconductor region. A gate oxide is then formed on the

exposed surface of the crystalline semiconductor region. The gate oxide serves as a gate insulation layer for a gate electrode formed on the gate oxide (Figures 2a to 2i; Spec. 8, 9, and 11 to 20).

Claim 1 is representative of the claimed invention, and it reads as follows:

1. A method of forming a field effect transistor, the method comprising:

forming an implantation mask over a crystalline semiconductor region;

forming a drain region and a source region adjacent said implantation mask, said drain and source regions each having a top surface located above a top surface of said crystalline semiconductor region;

removing said implantation mask to expose a surface area of said top surface of said crystalline semiconductor region;

forming a gate insulation layer on said exposed surface area of said top surface of said crystalline semiconductor region;

forming a gate electrode on said gate insulation layer; and

doping said gate electrode.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Chan	US 6,252,277 B1	Jun. 26, 2001
Gardner	US 6,355,955 B1	Mar. 12, 2002

The Examiner rejected claims 1 to 4, 9 to 15, 21 to 23, and 25 to 32[1] under 35 U.S.C. § 102(b) based upon the teachings of Chan.

[1] Although the opening statement of the rejection does not list claim 32 (Ans. 3), it is clear in the body of the rejection that claim 32 was included in the rejection (Ans. 9).

The Examiner rejected claims 5 to 8 under 35 U.S.C. § 103(a) based upon the teachings of Chan and Applicants' admitted prior art disclosed on pages 1 to 8 of the specification and figures 1a to 1d of the drawings.

The Examiner rejected claim 24 under 35 U.S.C. § 103(a) based upon the teachings of Chan and Gardner.

Turning first to the anticipation rejection, the Examiner contends *inter alia* that Chan teaches "forming drain and source regions (39) adjacent said implantation mask (37) (figure 4E)," and "removing said implantation mask (37) to expose a top surface area of said crystalline semiconductor region (30)" (Ans. 4). Appellants contend that the source and drain regions in Chan are not formed "adjacent" to the implantation mask 37 because of the presence of the spacers 35 between the implantation mask 37 and the source and drain regions (Br. 7). Appellants also contend that the bottom of trench 36 in Chan is not the "top surface" of the crystalline semiconductor region (Br. 8).

Chan describes a method of fabricating a field effect transistor that comprises the steps of forming an implantation mask 37 (i.e., undoped silicon oxide) over field oxide 32 and spacers 35 that are formed on the top surface of crystalline semiconductor region 30 (Figs. 4B and 4C). The implantation mask 37 fills trench 36 formed in crystalline semiconductor region 30 (Fig. 4C). After removal of the implantation mask 37 from the top surface of the crystalline semiconductor region 30 (Fig. 4D), a drain region 39 and a source region 39 are formed adjacent spacers 35 on the top surface of the crystalline semiconductor region 30 (Fig. 4E; col. 5, ll. 7 to 17). The drain region 39 and the source region 39 each have a top surface located above the top surface of the crystalline semiconductor region 30 (Fig. 4E). The silicon oxide implantation mask 37 that remains in the trench 36 is

removed to expose the sidewalls of the trench and the floor of the trench (Fig. 4F; col. 5, ll. 18 to 56). A gate insulation layer 44 is then formed on the exposed surface area of the trench floor in the crystalline semiconductor region 30 (Fig. 4G; col. 5, ll. 57 to 61). Thereafter, a doped gate electrode 47 is formed on the gate insulation layer 44 (Figs. 4H and 4I; col. 6, ll. 20 to 24).

In view of the noted teachings by Chan, we agree with the Appellants that the drain and source regions 39 are formed "adjacent" the spacers 35 as opposed to the implantation mask 37 in the trench 36. The presence of the spacers 35[2] prevents the drain and source regions 39 from sharing a common border with the implantation mask 37. We also agree with the Appellants that the gate insulation layer 44 and the gate electrode 47 in Chan are formed in the trench 36 formed in the crystalline semiconductor region 30, and are not formed on the "top surface" of the crystalline semiconductor region. Thus, the anticipation rejection of claims 1 to 4, 9 to 15, 21 to 23, and 25 to 32 is reversed because each and every limitation in the claims is not found either expressly or inherently in the cited reference to Chan. *In re Crish*, 393 F.3d 1253, 1256 (Fed. Cir. 2004).

Turning to the obviousness rejections of claims 5 to 8 and 24, these rejections are reversed because the teachings of Appellants' admitted prior art and Gardner do not cure the noted shortcomings in the teachings of Chan, and because the Examiner's articulated reasons for combining the teachings of Appellants' admitted prior art and Gardner with those of Chan do not

[2] If air spaces were used by Chan in lieu of a spacer material, then we would agree with the Examiner that the drain and source regions would be adjacent the implantation mask.

support a legal conclusion of obviousness. *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1741 (2007).

The decision of the Examiner is reversed.

REVERSED

gvw

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